What is claimed is:

1. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

   applying a programming voltage to a first word line coupled to a control gate of the selected memory cell, wherein a gate/source voltage equal to the programming voltage is sufficient to cause a reversal of polarity of each memory cell;

   applying a fraction of the programming voltage to other word lines coupled to control gates of non-selected memory cells not associated with the first word line;

   applying a ground potential to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell; and

   applying the fraction of the programming voltage to other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line and to other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line.

2. The method of claim 1, wherein the programming voltage is approximately 6V.

3. The method of claim 1, wherein the fraction of the programming voltage is approximately 1/2.

4. The method of claim 1, wherein a gate/source voltage equal to fraction of the programming voltage is sufficient to cause a reversal of polarity of each memory cell.

5. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a programming voltage to a first word line coupled to a control gate of the selected memory cell, wherein a gate/source voltage equal to approximately 1/3 the programming voltage is sufficient to cause a reversal of polarity of each memory cell;

applying approximately 1/2 the programming voltage to other word lines coupled to control gates of non-selected memory cells not associated with the first word line;

applying a ground potential to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell; and

applying approximately 1/2 the programming voltage to other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line and to other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line.

6. The method of claim 5, wherein the programming voltage is approximately 6V.

7. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a ground potential to a first word line coupled to a control gate of the selected memory cell;

applying a fraction of a programming voltage to other word lines coupled to control gates of non-selected memory cells not associated with the first word line, wherein a gate/source voltage equal to the programming voltage is sufficient to cause a reversal of polarity of each memory cell;

applying the programming voltage to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell; and

applying the fraction of the programming voltage to other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line and to other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line.

8. The method of claim 7, wherein the fraction of the programming voltage is approximately 1/2.

9. The method of claim 7, wherein the programming voltage is approximately 6V.

10. The method of claim 7, wherein a gate/source voltage equal to the fraction of the programming voltage is sufficient to cause a reversal of polarity of each memory cell.

11. The method of claim 7, wherein applying the ground potential to the first word line and applying the programming voltage to the first program line and to the first bit line when the selected cell has a data value of 1 causes the selected cell to reverse its polarity.

12. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a ground potential to a first word line coupled to a control gate of the selected memory cell;

applying approximately 1/2 a programming voltage to other word lines coupled to control gates of non-selected memory cells not associated with the first word line, wherein a gate/source voltage equal to approximately 1/3 the programming voltage is sufficient to cause a reversal of polarity of each memory cell;

applying the programming voltage to a first program line coupled to a first source/drain region of the selected memory cell and to a first bit line coupled to a second source/drain region of the selected memory cell; and

applying approximately 1/2 the programming voltage to other program lines coupled to first source/drain regions of non-selected memory cells not associated with the first program line and to other bit lines coupled to second source/drain regions of non-selected memory cells not associated with the first bit line.

13. The method of claim 12, wherein the programming voltage is approximately 6V.

14. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a programming voltage to a first word line coupled to a first row of the array;

applying a fraction of the programming voltage to other word lines respectively coupled to other rows of the array;

applying a ground potential to a first program line coupled to a first column of the array and to a first bit line coupled to the first column of the array; and

applying the fraction of the programming voltage to other program lines respectively coupled to other columns of the array and to other bit lines respectively coupled to the other columns of the array;

wherein the selected memory cell is located in the first row and first column of the array at an intersection of the first bit line and first word line, the change in the voltage across the selected memory cell substantially equal to the programming voltage and sufficient to cause a reversal of polarity of the selected memory cell.

15. The method of claim 14, wherein a change in a voltage across other memory cells of the first column of the array is a fraction of the programming voltage and a change in a voltage across other memory cells of the first row of the array is a fraction of the programming voltage.

16. The method of claim 15, wherein a change in a voltage across memory cells of the other rows and columns is substantially zero.

17. The method of claim 14, wherein a change in a voltage across other memory cells of the first column of the array is not sufficient to cause a reversal of polarity of those memory cells, a change in a voltage across other memory cells of the first row of the array is not sufficient to cause a reversal of polarity of those memory cells, and a change in a voltage across memory cells of the other rows and columns is not sufficient to cause a reversal of polarity of those memory cells.

18. A method of writing to a selected ferroelectric memory cell in an array of ferroelectric memory cells, the method comprising:

applying a ground potential to a first word line coupled to a first row of the array;

applying a fraction of a programming voltage to other word lines respectively coupled to other rows of the array;

applying the programming voltage to a first program line coupled to a first column of the array and to a first bit line coupled to the first column of the array; and applying the fraction of the programming voltage to other program lines respectively coupled to other columns of the array and to other bit lines respectively coupled to the other columns of the array;

wherein the selected memory cell is located in the first row and first column of the array at an intersection of the first bit line and first word line, the change in the voltage across the selected memory cell is sufficient to cause a reversal of polarity of the selected memory cell.

19. The method of claim 18, wherein a change in a voltage across other memory cells of the first column of the array is not sufficient to cause a reversal of polarity of those memory cells, a change in a voltage across other memory cells of the first row of the array is not sufficient to cause a reversal of polarity of those memory cells, and a change in a voltage across memory cells of the other rows and columns is not sufficient to cause a reversal of polarity of those memory cells.